Synthesis of Edge-Closed Graphene Ribbons with Enhanced Conductivity

Woo Jong Yu,[†] Sang Hoon Chae,[†] David Perello,[‡] Si Young Lee,[†] Gang Hee Han,[†] Minhee Yun,[‡] and Young Hee Lee[†,*]

[†]Sungkyunkwan Advanced Institute of Nanotechnology, Department of Physics, Department of Energy Science, Center for Nanotubes and Nanostructured Composites, Sungkyunkwan University, Suwon 440-746, Korea, and [‡]Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania 15261

ABSTRACT Edge-closed and edge-opened graphene ribbons were synthesized on Pd nanowire templates using plasma-enhanced chemical vapor deposition (PECVD). After metal nanowire etching, the tubular shaped thin graphene layers were collapsed to edge-closed graphene ribbon. In order to make edge-opened graphene ribbons, the graphene layers on the top part of the metal nanowire were selectively etched by O_2 plasma. The protected graphene layers at the bottom of nanowire are transformed to edge-opened graphene ribbon after nanowire etching. Because of defect-free edges, edge-closed graphene ribbon showed reduced D-band intensity compared to edge-opened graphene ribbons, and moreover, the conductivity of edge-closed graphene ribbon was much higher than that of edge-opened graphene ribbon.

A single graphene layer has been demonstrated to generate high mobility (15 000 cm^2 V^{-1} s^{-1}) and the quantum Hall effect at room temperature.[1−7] Graphene nanoribbon (GNR), a thin and elongated strip of graphene, displays semiconductor or semi-metal properties depending on its width and edge type.[8,9] Several methods to produce GNRs such as electron beam lithography,[10,11] physical and chemical processes,[12−17] unzipping of carbon nanotubes,[18−22] and chemical vapor deposition[23,24] have been developed. However, controlling the widths and lengths of the GNRs is one of the main obstacles to their application to devices. E-beam lithography has been used to fabricate individual GNRs, allowing control of width and length, but is not amenable to high density device integration. On the other hand, unzipping and chemical vapor deposition generate a reasonable amount of GNRs, but control of the diameter and length has not been realized using these processes. Even though the GNRs were produced, edge-opened GNRs are more vulnerable to defects than carbon nanotubes.[25,26] In fact, graphene edges showed much more defects than the bulk of graphene sheets.[27] It has been predicted from theory that these defects at the edges significantly influence degradation of electrical conductivity.[28]

Here, we report a facile synthesis method for edge-closed GRs (ECGRs) and graphene tubes (GTs) using Pd nanowire templates. The obtained ECGRs and GTs demonstrated monodispersed diameters and lengths, where the diameter was determined by the pore sizes of the anodic alumina and the length was determined by the electrochemical deposition time. The GTs were obtained by retaining their tubular shape when thick graphene layers were formed. On the other hand, the ECGRs were obtained by collapsing their tubular shape into sheets after metal nanowire etching when thin graphene layers were formed. The ECGRs removed the parasitic defects on the edge side, and thus resulted in higher conductivity than edge-opened GRs (EOGRs), while revealing semiconducting transport behavior.

A schematic of the procedure used to make the ECGRs and GTs is shown in Figure 1. Pd nanowire-dispersed solution was sprayed on a Si/SiO$_2$ substrate (Figure 1a). The substrate was placed into the PECVD chamber, and the graphene layers were grown on the Pd nanowire template (Figure 1b). The ECGRs and GTs were obtained by selective etching of the Pd nanowires within the dilute HNO$_3$ (Figure 1c,d). The thick graphene layers retained their tubular shape and formed GTs (Figure 1c). On the other hand, thin graphene layers were folded into a sheet and formed ECGRs after removal of Pd supporter (Figure 1d). In order to compare the conductivity of ECGRs and EOGRs, EOGRs were constructed by a further process. The graphene layers on the
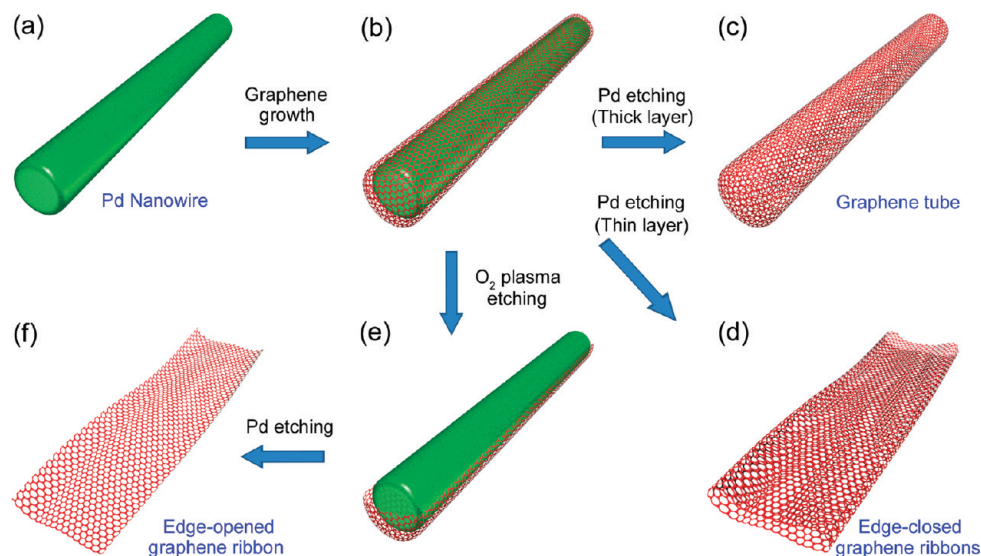
Figure 1. Schematic of the process used to fabricate ECGRs, GTs, and EOGRs. (a) Pd nanowire synthesized through porous alumina template by electrodeposition, (b) graphene layer growth on the Pd nanowire surface, (c) GTs with thick layers, (d) ECGRs with thin layers after etching of the Pd nanowires, (e) O_2 plasma etching of the top half of the graphene layer, and (f) EOGRs formed by etching the remaining Pd nanowires on (e).

top part of the Pd nanowire were selectively etched by O_2 plasma (Figure 1e). O_2 plasma is a well-known approach for etching carbon structures.[30] O_2 plasma affects only the front side of the Pd nanowires, and as a consequence, the half cylinder (top part) of the graphene can be selectively etched. The other half (bottom part) of the graphene layers behind the Pd nanowires was not attacked by O_2 plasma because of the protection from the plasma by the Pd nanowires. The EOGRs were finally obtained after etching of the Pd nanowires within dilute HNO_3 (Figure 1f).

Scanning electron microscopy (SEM) images for each fabrication step are shown in Figure 2. The alumina template was etched in 5 M NaOH solution for only about 5 min in order to etch an extra alumina template above the Pd nanowires. Figure 2a shows vertically grown Pd nanowires through the alumina pores. The Pd nanowires grown by this method have uniform height and diameter. The alumina template was further etched by 5 M NaOH solution, and only Pd nanowires remained on the Au film (Figure 2b). The average diameter of the Pd nanowires was 250 nm, following the pore size of the alumina template. The small variance of the Pd nanowire diameters originated from the porous alumina prepared by a single-step anodization process. A uniform pore diameter could be obtained if double-step anodized alumina was used as a template.[31] Similarly, the diameters of the pores in the alumina can also be controlled, which provides controllability of the Pd nanowires.[29] The Au film with Pd nanowires was dipped in deionized water and sonicated to detach the Pd nanowires from the Au substrate and to generate better dispersion. Figure 2c−h shows the SEM images of the ECGRs and GTs synthesized on the Pd nanowires by PECVD. The graphene lay-

ers were uniformly grown over the Pd nanowires (Figure 2c−e). A transparent thin graphene layer was covered on the outside of the Pd nanowires (bright
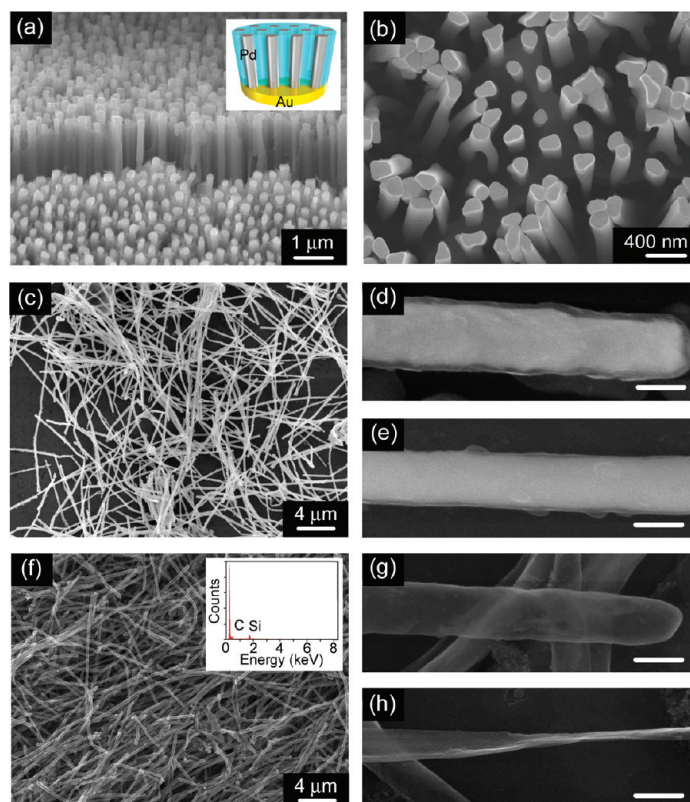

Figure 2. SEM images of (a) Pd nanowires grown through the alumina pores with the inset showing a schematic; (b) vertically aligned Pd nanowires after the alumina template was removed; (c) graphene layer grown Pd nanowires separated from the Au substrate, magnified Pd nanowires with (d) thick graphene layers and (e) thin graphene layers; (f) hollow graphene layers after etching of the Pd nanowires with the inset corresponding to the EDX spectrum; and (g) GTs and (h) ECGRs the corresponding of (d) and (e) after Pd etching, respectively. The scale bars in (d), (e), (g), and (h) are 200 nm.
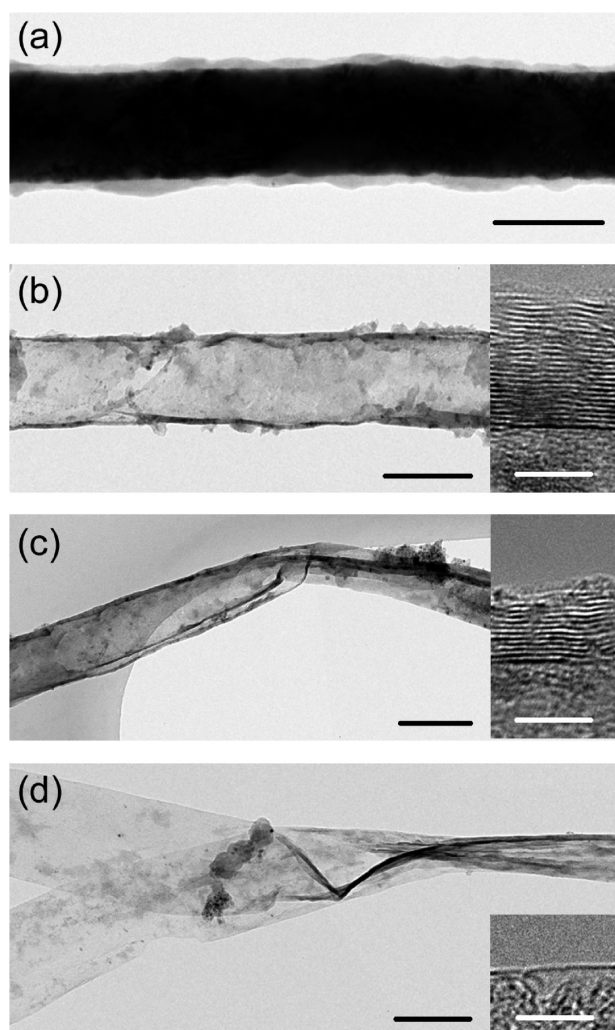
Figure 3. TEM images of (a) synthesized graphene on Pd nano-wires, (b) graphene layers with 23 layers, (c) 11 layers, and (d) single layer after etching of Pd nanowires. Insets of (b−d) are high-resolution TEM images of walls at the edge of GTs and ECGRs. The scale bars of (a−d) are 200 nm and insets of (b−d) are 5 nm.

Figure 4. SEM images of (a) Pd nanowires with partially re-maining graphene layers (bottom side) treated by O_2 plasma etching and (b) the remaining EOGRs after etching the Pd nanowires. (c) Raman spectra of ECGR and EOGR. The scale bars are 200 nm in (a) and 300 nm in (b) and (c).

color), as seen in Figure 2d,e. The hollow graphene lay-ers remained after etching of Pd nanowires by dilute HNO_3 (Figure 2f−h). The inset in Figure 2h displays the energy-dispersive X-ray spectrum (EDX) taken from the sample in Figure 2f. The EDX shows only carbon and sili-con peaks without a Pd peak. This spectrum means ro-bust etching of the Pd nanowires inside the graphene layers. The graphene layers after removal of opaque Pd nanowires were transparent, and other graphene lay-ers were visible through the overlapped graphene lay-ers (Figure 2g,h). The average diameter of the hollow graphene layers was 250 nm, which is almost the same as that of Pd nanowires. The thickness of the graphene layers varied by the amount of C_2H_4 gas while growing the graphene layers (described in the Methods). The thick graphene layers shown in Figure 2d sustained their tubular shape and formed GTs after Pd etching (Figure 2g). On the other hand, the thin graphene lay-ers seen in Figure 2e were too weak to maintain the tu-bular shape. They were folded to yield a ribbon, ECGR,
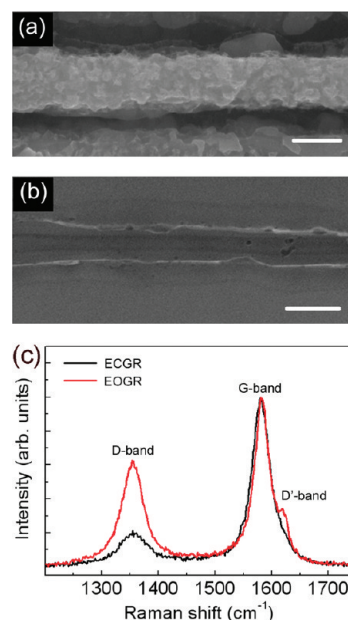
after Pd etching (Figure 2f). This folding occurred by a strong surface tension of the graphene during wet etching.

The TEM image provides further insight into the structure and the number of walls of the ECGRs and GTs. Figure 3a shows Pd nanowires (dark area) uni-formly covered with graphene layers after growing the graphene layers (white on the surface). Pd core region was removed by wet etching, and then hollow graphene layers were left exclusively (Figure 3b−d). De-pending on the number of layers, different morpholo-gies were observed. The thickness of the graphene lay-ers in Figure 3b was about 8 nm, corresponding to 23 layers. At this thickness, the tubular structure of the graphene layers was maintained without deformation, and as a consequence, GTs were formed. In Figure 3c, however, the thickness of the graphene layers was 4 nm, corresponding to 11 layers. In this case, the tubu-lar shape was folded in some portion, and the ECGRs were formed. In the case of a single graphene layer, some parts were easily torn out and corrugated severely (Figure 3d).

In order to compare the defects and conductivities of ECGRs and EOGRs, EOGRs were constructed by an ad-ditional process. O_2 plasma etching is known to gener-ate the EOGRs. The Pd nanowires with graphene layers were placed in an O_2 plasma chamber. The top graphene layers and part of the Pd nanowires were etched away, leaving a corrugated Pd nanowire sur-face, as shown in Figure 4a. The Pd nanowires acted as a rod mask to protect the graphene layers underneath the Pd nanowires during the plasma etching. The par-tially etched graphene layers were dipped in dilute
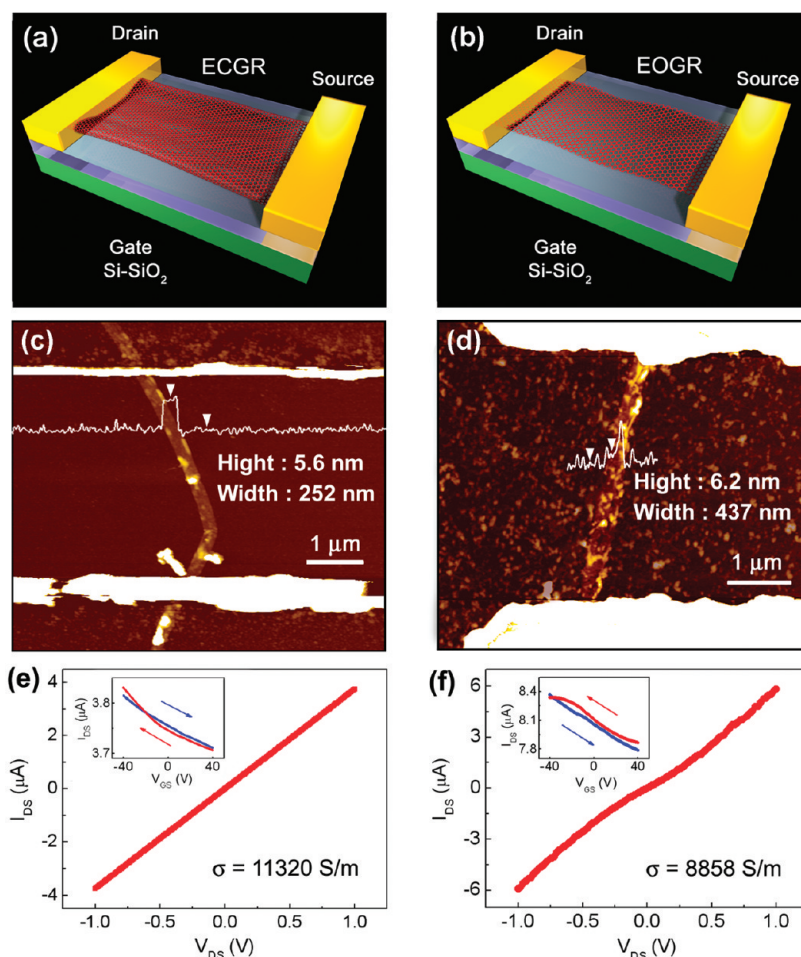
Figure 5. Three-dimensional schematics of the (a) ECGR-FET and (b) EOGR-FET with a silicon back gate. AFM image of (c) ECGR-FET and (d) EOGR-FET. The channel width is 4 μm. Electrical characteristics of (e) ECGR-FET and (f) EOGR-FET at zero gate bias with insets of transfer characteristics.

HNO_3 to etch away the Pd nanowires. The remaining EOGRs are shown in Figure 4b. The bulk region of EOGRs was smooth due to the protection by the Pd nanowires. However, the edges of EOGRs were very rough because of O_2 plasma attraction. This edge roughness is in contrast with ECGRs. In order to compare the amount of defects, we measured micro-Raman spectroscopy. The laser spot size of 1 μm was enough to measure bulk and edges of graphene layers. The D-band of EOGRs was much higher than that of ECGRs in the Raman spectra (Figure 4c). This means that defects were formed at the edge side during plasma etching process. The formation of defects at the edge can be also confirmed by the new appearance of D′-band near 1620 cm^{-1}, which is associated with defects created during oxygen plasma treatment, in good agreement with the previous result.[32]

The electrode was deposited after spray ECGR and EOGR on the substrate in order to reduce contact resistance by surrounding the ECGR and EOGR with electrode.[33] Figure 5c shows the AFM image of ECGR field effect transistor (FET). Single ECGR was located between a source and drain electrode for the channel.

The ECGR has a width of 252 nm, a height of 5.6 nm, and a length of 4 μm. On the order hand, the AFM image of EOGR is shown in Figure 5d, where the EOGR has a width of 437 nm, a height of 6.2 nm, and a length of 4 μm. The substrate had a rough surface in this case due to O_2 plasma etching. Figure 5e,f shows $I-V$ characteristics of ECGR and EOGR. The measured conductivity of $\sigma = 11320$ S/m of ECGR at zero gate bias is much higher than $\sigma = 8858$ S/m of EOGR. The high conductivity of ECGR is attributed to the defect-free edges confirmed from Raman spectra in Figure 4. The inset of Figure 5e,f shows small p-type gate dependence of both ECGR and EOGR. This was ascribed to ambient air.[34]

Figure 6a,b shows the $I-V$ characteristics of ECGR associated with temperature changes. Figure 6c−e shows the temperature-dependent $G = dI/dV$ and resistivity 30 K $< T <$ 300 K. The data indicate two regimes, one (30−150 K) with very weak power-law dependence and the other (150−300 K) with linear temperature dependence. The high-temperature regime dependence is attributed to phonon-enhanced conductance, for example, an enhancement in the conductance due to phonon-assisted tunneling either near the contacts or through
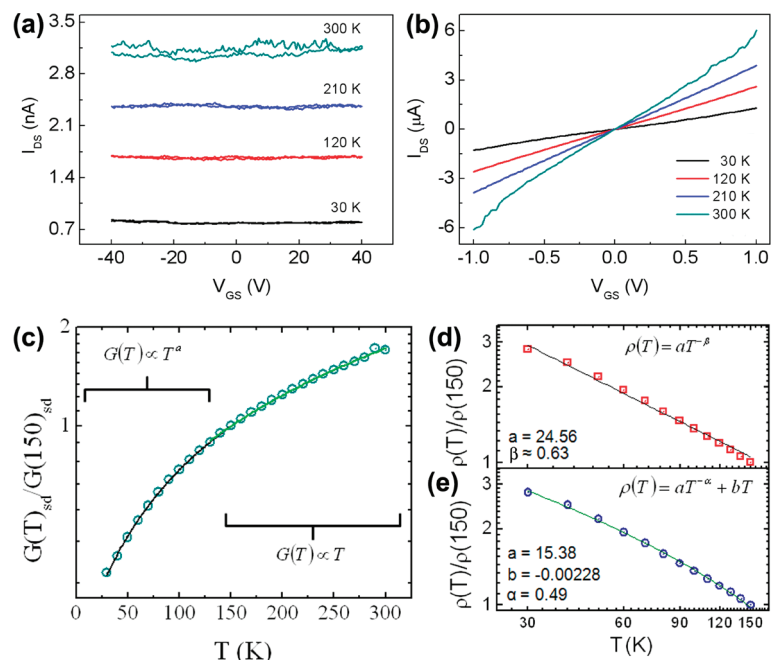
Figure 6. (a) Source−drain current of ECGR as a function of gate voltage (V_{SD} = 1 mV) and (b) I_{SD} *versus* V_{SD} of ECGR (V_{GS} = 0) measured at different temperatures under vacuum. (c) Temperature-dependent G = dI/dV indicating two transport regimes for 30 K < T < 150 K (electron−electron + electron−phonon) and 150 K < T < 300 K (electron−phonon). (d) Fitting to simplified power-law temperature dependence matches poorly to experimental observation while the addition of a linear term (e) improves fitting and suggests enhanced conductance from electron−phonon interactions.

grain edges and defect site induced traps in the ECGR. These disorder sites overshadow the electron−electron (coulomb) interactions for the temperature and bias regimes investigated. Figure 6d shows the weak fitting with a simplified (ignorant of differences between disorder, umklapp, and other mechanisms) power-law transport model to the version proposed by Kane *et al.* for resistance of temperature region one.[35] However, more success is achieved using a combination of the power-law (electron−electron) and linear (phonon−electron) terms in Figure 6e. The negative coefficient on the linear term indicates that as phonon scattering is decreased with temperature (phonon population is proportional to temperature[36]) fewer carriers tunnel through and out of disorder regions. Thus the resistance shows increasingly weak linear dependence and signs of increasingly interacting electrons as temperature decreases.

In summary, edge-closed graphene ribbons and graphene tubes were synthesized by graphene sheet growth on a Pd nanowire template using PECVD. This process provides an easy and convenient method for producing edge-closed graphene ribbons and graphene tubes with uniform thicknesses and lengths. More than 20 graphene layers constructed graphene tubes, while less than 20 graphene layers formed edge-closed graphene ribbons. The closed edges reduced parasitic defects at the edge region, resulting in improvement of conductivity. Temperature-dependent electrical measurements indicate that transport is phonon-assisted at high temperature and resembles a weakly interacting Lüttinger liquid at temperatures closer to 30 K. We expect that the edge-closed graphene ribbons will provide uniform conducting paths in flexible nanoscale devices with high conductivity. Furthermore, graphene tubes with large surface area and large inner room can be utilized as a storage material and drug delivery.

METHODS

Pd Nanowire Synthesis. Pd nanowires were synthesized using an electrochemical deposition method.[29] Gold was deposited by a thermal evaporator on one side of a Al_2O_3 template (Whatman Co.). $Pd(NH_3)_4Cl_2$ (10 g/L) and NH_4Cl (20 g/L) were dissolved in deionized water for the Pd electrolyte solution. The Au-deposited portion of the Al_2O_3 template was attached to the Cu electrode and dipped in an electrolyte solution with a counter electrode of Pt wire. In order to electrodeposit the Pd within the pores of the Al_2O_3 template, a bias current of 10 mA was applied between the Cu electrode (negative) and the Pt wire electrode (positive) for 60 min. After synthesis of the Pd nanowires,

the Al_2O_3 template was removed by dipping in a 5 M NaOH solution. The Pd nanowires were washed with deionized water to remove the NaOH. Finally, the Pd nanowires were sonicated in deionized water for 10 min for dispersion. The diameter of the Pd nanowires is determined by the alumina pore size, and the length depends on the deposition time.[29]

Edge-Closed and Edge-Opened Graphene Ribbon Synthesis. Pd nanowires dispersed in deionized water were sprayed on a p-type doped Si/SiO_2 (300 nm) substrate. The prepared substrate was placed in a plasma-enhanced chemical vapor deposition (PECVD) chamber. The initial vacuum was maintained at 2 mTorr. The chamber was heated to 750 °C without gases as Pd nanowires deform at temperatures above 750 °C. When the temperature

reached 750 °C, 100 sccm of H_2 gas was flowed through the chamber with a plasma power of 100 W for 5 min to reduce the oxidized Pd on the Pd nanowire surface. Graphene layers were synthesized under gas flow rates of 40 sccm C_2H_4 (thick graphene layers) and 10 sccm (thin graphene layers) and 100 sccm H_2 with a plasma power of 300 W for 5 min. At a flow rate of 40 sccm C_2H_4, the graphene layers varied from 10 to 30 layers. On the other hand, the graphene layers were lower than 10 layers at 10 sccm C_2H_4. The chamber was cooled without gas supply at the end of the process. The grown graphene layers on the Pd nanowires were dipped in dilute HNO_3 for 12 h to selectively remove the Pd nanowires. The graphene layers were rinsed with deionized water. To synthesize EOGRs, O_2 plasma etching was further applied under an initial vacuum of 2 mTorr. Oxygen gas (1 sccm) and Ar gas (10 sccm) were flowed into the chamber for 90 min at a plasma power of 70 W.

Measurements. Further insight into the structure and the number of layers were obtained by a transmission electron microscope (TEM: JEM2100F, ZEOL). In order to prepare the samples for the TEM, ethanol was dropped on the ECGR and EOGR sprayed substrates. Few ECGRs and EOGRs were transferred to the TEM grid, when rubbing the substrate by a copper TEM grid.

The source and drain were patterned by photolithography on the ECGR and EOGR sprayed Si/SiO$_2$ wafer covered with photoresist (PR). The metals of Cr (5 nm)/Au (50 nm) were deposited by an e-beam evaporator at 2×10^{-6} Torr. The PR was lifted off with metals, and the remaining metals were formed for source and drain electrodes. The electrical characteristics of the ECGR-FET and EOGR-FET were measured under ambient conditions by source measure units (Keithley 236, 237) using a probe station. Low-temperature $I-V$ measurement was performed in the closed cycle refrigerator at the temperature range from 30 to 300 K in 3 mTorr.

Scanning electron microscope (JEOL, JSM-7401F) images were taken by secondary electron image mode under a pressure of $\approx 4 \times 10^{-3}$ Torr. The wavelength of resonant Raman spectroscopy (RM1000 microprobe; Renishaw) was 514 nm (2.41 eV). A Rayleigh line rejection filter with a spectral range of $70-3600$ cm^{-1} for Stokes shift was utilized to characterize the ECGR and EOGR.

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